18.7 A 10Gb/s CMOS CDR and DEMUX IC with a Quarter-Rate Linear Phase Detector

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High-speed CDR ICs, operating over 10Gb/s, are implemented by using a binary phase detector (PD) or a linear PD [1-3]. The gain of a binary PD depends on jitter amplitudes of input data and recovered clock. Therefore, the binary PD is not suitable for applications such as an OC-192 receiver that require accurately controlled loop bandwidth, unless a gain stabilization technique is used [1]. A linear PD, on the other hand, has a well-defined gain, but gives narrow phase error pulses (up/down pulses) to a charge pump (CP) even if a half-rate linear PD is adopted [2]. The proposed 10Gb/s CDR/DEMUX IC employs a quarter-rate linear PD. By latching and manipulating input data with 4 phase clocks from a quarter-rate LC-QVCO, the pulse width of the phase error is doubled, therefore, the required f_T and power consumption are reduced. The implemented IC consumes 640mW.

Figure 18.7.1 shows the block diagram of the 10Gb/s CDR/DEMUX IC. The CDR utilizes a dual-loop architecture that consists of a frequency-acquisition loop and a PLL [3]. After frequency acquisition reaches within ±400ppm, the lock controller sets the MUX to turn on a PLL. The PLL includes the quarter-rate linear PD, a data recovery (DR) circuit, a transconductor (gm) circuit, a loop filter, and a 4-phase 2.5GHz LC-QVCO. After a 4:16 DEMUX, 16b parallel data and 2 clock signals are fed to 18 LVDS drivers for I/O interface. Additionally, a loss of signal (LOS) indicator detects the input data by comparing the signal strength of the input data with a programmed threshold.

Figure 18.7.2 shows the block diagram and timing diagram of the proposed quarter-rate linear PD. The PD core consists of 4 latches, 4 XOR gates, and 8 AND gates; all CML types for high-speed operation. After latching input data by 4 phase recovered clocks separately, each latch output is XORed side by side and ANDed twice. As shown in the timing diagram, there are 4 up pulses, UP[3:0], and 4 down pulses, DN[3:0], with pulse widths of 150ps and 100ps, respectively. Since the rising edge of up pulses is triggered by data transition and the falling edge is triggered by clock transition, the pulse width is increased if the recovered clock transits behind the center of input data and decreased otherwise. For down pulses, however, both edges are triggered by clock transition and the pulse width is kept constant. The delay time through gates is compensated by designing a clock buffer with the same latches and gates before the recovered clocks drive the AND gates.

The configuration of the implemented DR is shown in Fig. 18.7.3. Here, the input signals, A, B, C and D, are from the latches of the PD, thus, there is no systematic timing skew between phase detection and data recovery. The recovered data, DATA[3:0], are all aligned synchronously with a phase of the recovered clock, CLK180, by passing through different numbers of latches. The latch cell in a 1.2V supply is implemented with a stacked architecture where DC bias comes from a replica bias circuit. By flowing a very small current (below the threshold current, I_{th}) through MP1 and MN2, the Vgd of MN1 is equal to the Vgs of MN2 ($<V_{th}$), which means MN1 is in saturation mode. Because the sizes of MN1-MN4 are the same, MN3 and MN4 operate also in saturation mode allowing reduced clock swing and fast switching time.

The phase error pulses from the PD are converted to current before entering the loop filter. In this gm circuit, there are 4 up paths and 4 down paths receiving UP[3:0] and DN[3:0] from the PD, respectively. Since the pulse width of up pulses is 150ps and that of down pulses is 100ps, the current mirror ratio is 2/3 for up pulses and 1 for down pulses as shown in Fig. 18.7.4. The up paths push the current to the loop filter according to the up pulses. However, to pull the current from the loop filter, the down paths are configured as complementary to the up paths with a source follower for DC level shifting. Since up/down pulses have different pulse widths and pass through different paths, there may exists static current mismatch in up/down paths. This current mismatch is digitally compensated by a 3b control word, gm_CTRL[2:0].

The on-chip 2.5GHz LC-QVCO generates 4 phase clocks. By using large coupling transistors between 2 LC tank oscillators, the phase error of the clocks is kept low not to degrade jitter performance even if LC mismatch exists. For a low duty ratio distortion, a clock buffer with AC coupling [4] is implemented. The frequency band of the LC-QVCO is selected by a 2b control word, LCVCO_BAND[1:0], for low VCO gain and multiple bit rates. The VCO shows a phase noise of -110dBc/Hz at 1MHz offset while consuming 10mA from a 1.2V supply including the clock buffer.

A binary tree structure is used for the 4:16 DEMUX. After being de-multiplexed, the 16b recovered data, DOUT[15:0], and 2 recovered clocks, RXPOCLK and RXMCLK, are fed to 18 preamplifiers and LVDS drivers. Each preamplifier and LVDS driver consumes 1mA and 10mA from a 2.5V supply, respectively. Timing skew between 622.08MHz RXPOCLK and 622.08Mb/s DOUT[15:0] is <140ps, which satisfies the OIF specification [5] as shown in Fig. 18.7.5.

Figure 18.7.6 shows the measured jitter tolerance of the CDR/DEMUX IC. For all measurements, 9.95Gb/s 2^{31}-1 PRBS is used. The Jitter tolerance is more than 0.5UIpp over 4MHz, exceeding the OC-192 requirements [6]. The sensitivity level is $210mV_{pp}$ and the measured BER is $<10^{-15}$. The jitter of the recovered clock, RXMCLK, is $2.1ps_{rms}$ and $15.6ps_{pp}$ at 155.52MHz. Multiple bit-rates are possible from 9.4 to 11.3Gb/s. Figure 18.7.7 shows a chip micrograph. The chip is fabricated in a 0.13μm 1P8M CMOS process and packaged in a 128 ball chip-array BGA. The die size is $10.2mm^2$ including on-chip I/O terminations, ESDs, and pads. Power consumption is 100mA from a 1.2V core supply and 205mA from a 2.5V I/O supply including 18 LVDS drivers.

References:

[1] B.-J. Lee, et al., "A 2.5-10Gb/s CMOS Transceiver with Alternating Edge-Sampling Phase Detection for Loop Characteristic Stabilization," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1821-1829, Nov., 2003.

[2] J. Savoj and B. Razavi, "A 10Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector," *IEEE J. Solid-State Circuits*, vol. 36, pp. 761-768, May, 2001.

[3] J. Cao, et al., "OC-192 Transmitter and Receiver in Standard 0.18-um CMOS," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1768-1780, Dec., 2002.

[4] J. Kim, et al., "A Four-channel 3.125Gb/s/ch CMOS Serial-Link Transceiver with a Mixed-Mode Adaptive Equalizer," *IEEE J. Solid-State Circuits*, vol. 40, pp. 462-471, Feb., 2005.

[5] "SFI-4 OIF-PLL-02.0 Proposal for a Common Electrical Interface Between SONET Framers and Serializer/Deserializer Parts for OC-192 Interfaces," *Optical Internetworking Forum*, OIF-SFI4-01.0, Sept., 2000.

[6] "Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria," *Telcordia Technologies*, GR-253-CORE, Sept., 2000.

 1-4244-0079-1/06/$20.00

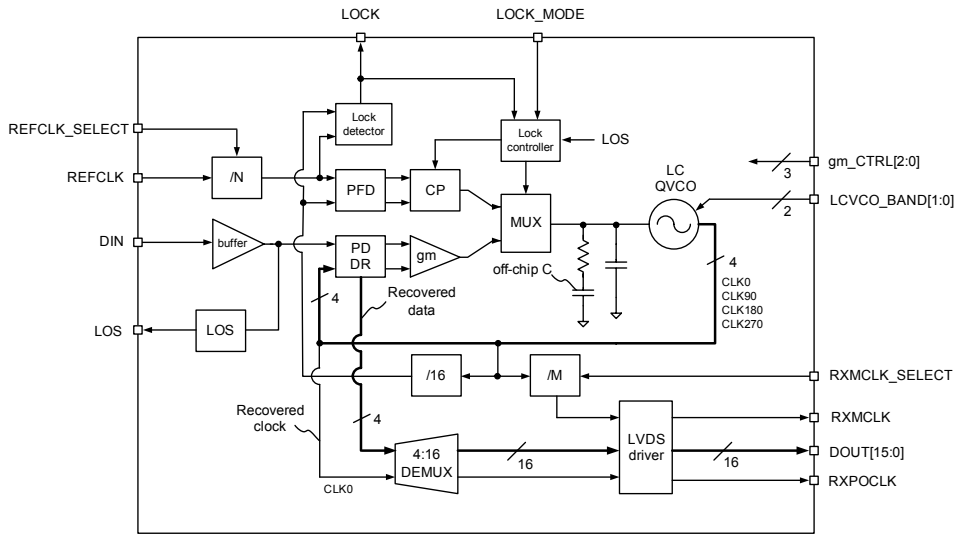


Figure 18.7.1: Block diagram of the 10Gb/s CDR/DEMUX IC.

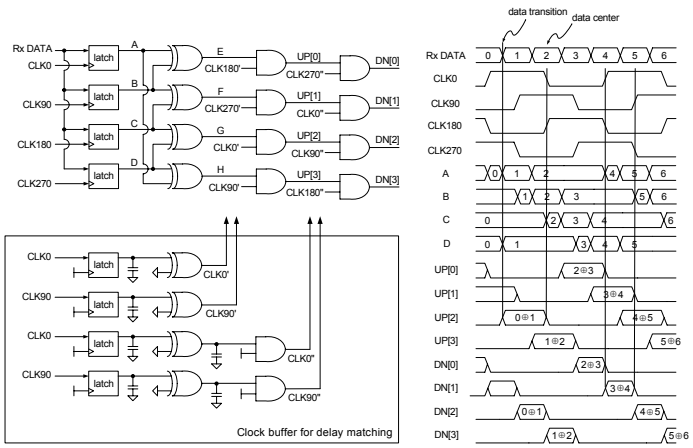


Figure 18.7.2: Block diagram and timing diagram of the proposed quarter rate linear PD

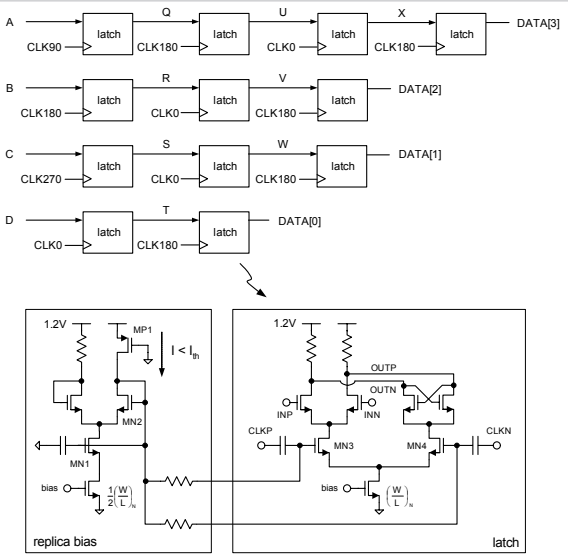


Figure 18.7.3: Data recovery circuit and latch schematic.

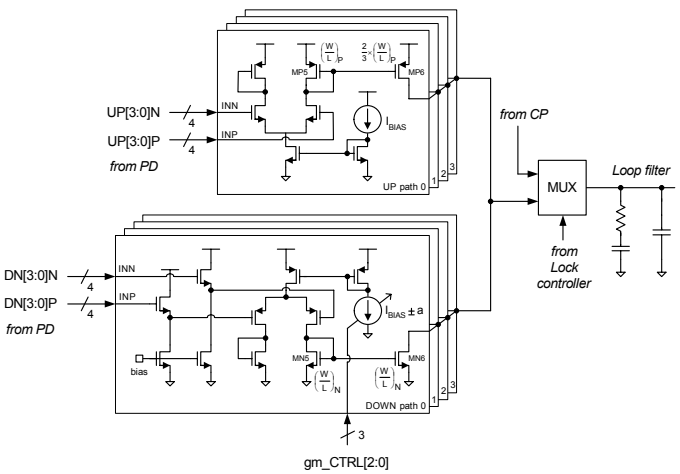
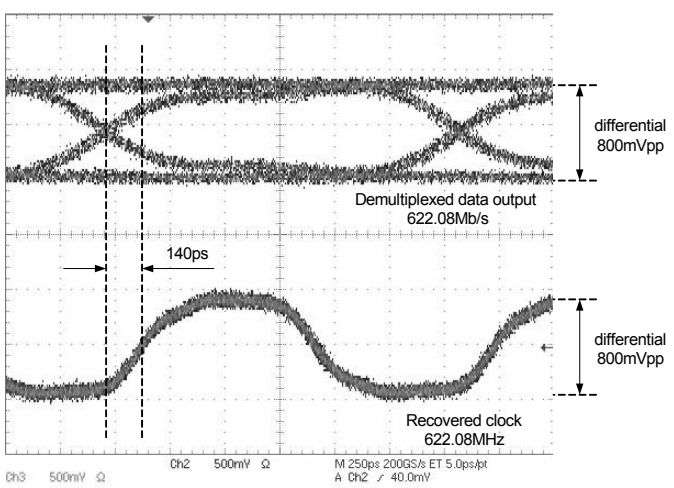


Figure 18.7.4: Block diagram of the transconductor circuit.



Horizontal scale = 250ps/div. and vertical scale = 500mV/div.

Figure 18.7.5: Demultiplexed data output (DOUT) and recovered clock (RXPOCLK).

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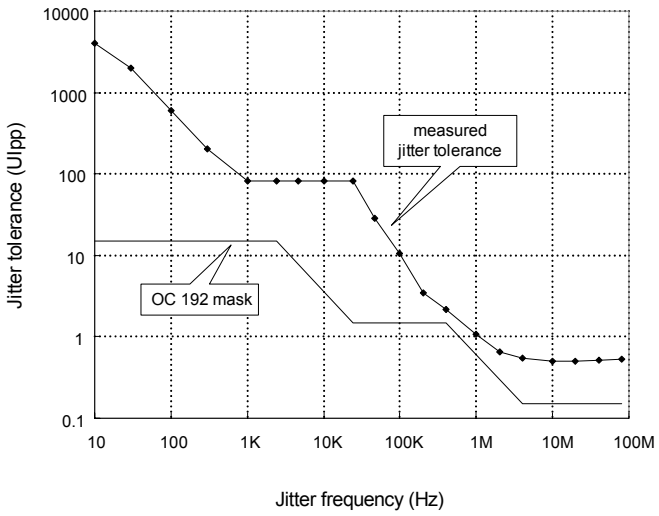

Figure 18.7.6: Measured jitter tolerance.

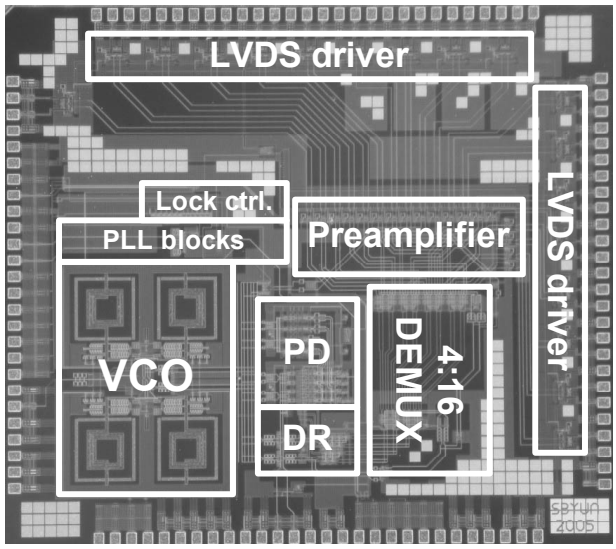

Figure 18.7.7: Chip micrograph.

